LCAU 2019 - SPI/SPIDEV for IoT

SPI/SPIDEV for IoT

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Brought to you by:

- Linux Foundation Training has provided speaker funding
- ARM is subsidizing the manufacturing of the floral bonnet for LCA2019
What is SPI?

- Serial Peripheral Interface
- Motorola
- de facto standard
- master-slave bus
- 4 wire bus
  - except when it’s not
- no maximum clock speed
- “A glorified shift register”

http://wikipedia.org/wiki/Serial_Peripheral_Interface
Common uses of SPI

- Flash memory
- ADCs
- Chromium Embedded Controller
- LCD Controllers
- Sensors
  - Thermocouples and other high data rate devices
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Advantages:

- Full Duplex in default mode
- Uses 4 pins (or 3 in some implementations)
- Low Processor overhead (even bit banged)
- No “unique address” needed (often just setting a GPIO pin to address)
- No “Protocol” to decode. (although can be used as transport for Protocols)
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Disadvantages:

● Higher pin count than i2c
● No in-band addressing (need HW pins to address)
● No slave ack that the data/command got to the intended recipient.
● No error checking
● Relatively short distances (often only onboard)
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SPI Signals

- MOSI - Master Output Slave Input
  - SIMO, SDI, DI, SDA
- MISO - Master Input Slave Output
  - SOMI, SDO, DO, SDA
- SCLK - Serial Clock (Master output)
  - SCK, CLK, SCL
- SS - Slave Select (Master output)
- CSn, EN, ENB
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SPI Master and Slave
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Master

Slave

Memory

0 1 2 3 4 5 6 7

SCLK

MOSI

MISO

0 1 2 3 4 5 6 7

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Basic SPI Timing Diagram
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SPI Modes

- Modes are composed of two clock characteristics
- CPOL - clock polarity
  - 0 = clock idle state low
  - 1 = clock idle state high
- CPHA - clock phase
  - 0 = data latched falling, output rising
  - 1 = data latched rising, output falling
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SPI Modes Cont’d

<table>
<thead>
<tr>
<th>Mode</th>
<th>CPOL</th>
<th>CPHA</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
SPI Mode Timing - CPOL 0

SPI Write Mode 0

Clock idle low, data latched on rising edge

SPI Write Mode 1

Clock idle low, data latched on falling edge
SPI Mode Timing - CPOL 1

Clock idle high, data latched on falling edge

Clock idle high, data latched on rising edge
Let’s look at an example together:

SPI can be more complicated

- **Multiple SPI Slaves**
  - One chip select for each slave
- **Daisy Chaining**
  - Inputs to Outputs
  - Chip Selects
- **Dual or Quad SPI (or more lanes)**
  - Implemented in high speed SPI Flash devices
  - Instead of one MISO, have N MISOs
  - N times bandwidth of traditional SPI
- **3 Wire (Microwire) SPI**
  - Combined MISO/MOSI signal operates in half duplex
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Multiple SPI Slaves
SPI Daisy Chain

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SPI Mode Timing - Multiple Slaves
Conclusions:

- Old Reliable Bus
- Still quite popular
- New variants are making it even more useful (QSPI, etc)